REMARKS/ARGUMENTS

The present amendment is submitted in response to the Office Action received from the United States Patent Office dated October 2, 2009. The Patent Office rejected Claims 1-11 under 35 U.S.C. §103(a) as being anticipated by *Hovell et al.* (U.S. Patent Number 7,116,681) in view of *Hies et al.* (U.S. Patent Number 7,333,510).

In response to the Office Action has amended Claims 1 and 7 to overcome the Examiner's rejections. Applicant respectfully submits that the amendments and the explanations below overcome the rejections to the claims. Applicant submits that all of the claims are now in condition for allowance. Notice to that effect is requested.

The Patent Office rejected Claims 1-11 under 35 U.S.C. §103(a) as being anticipated by *Hovell et al.* (U.S. Patent Number 7,116,681) in view of *Hies et al.* (U.S. Patent Number 7,333,510). The Patent Office states as to Claim 1, *Hovell et al.* discloses a communication protocol converter comprising: (a) a first modular communication jack having: a housing defining an open cavity and a segregated interior chamber, a connector port having a plurality of electrical contacts positioned within said open cavity, at least one circuit board incorporating Ethernet to raw data conversion circuitry components for a first communication protocol disposed within said interior chamber in electrical communication with the electrical contacts of said connector port; wherein the circuitry components are positioned on both sides of the at least one circuit board (ports connecting 62(A, B) and 72(A, B) of fig.2, see fig.2, col.8 line 10 to col.9 line 20); and iv) a memory positioned on said circuit board in electrical communication with said conversion circuitry for a first communication protocol for receiving converted data (using network controller to process data conversion, see figs.1, 2, col.6 line 13 to col.7 line 50); whereby the memory is interconnected to a bi-directional data line that allows the input and output of raw data (writing and accessing data from/to the storage (68A fig.2), see col.8 line 10 to col.9 line 20) (b) a second modular communication jack having: i) a housing defining an open cavity and a segregated interior chamber; ii) a connector port having a plurality of electrical contacts positioned within said open cavity; iii) at least one circuit board incorporating Ethernet to raw data conversion circuitry components for a second communication protocol disposed within said interior chamber in electrical communication with the electrical contacts of said

connector port; a memory positioned on said circuit board in electrical communication with said conversion circuitry for said second communication protocol for receiving converted data (see fig.2, col.7 line 17 to co1.8 line 58) wherein the memory is connected with the bi-directional line to receive input of raw data from the first modular communication jack; and (c) a bidirectional data interface electrically interconnecting said memory of said first communication jack with said memory of said second communication jack (processing data in/out of the storage, see co1.8 lines 10-58).

Hovell et al. does not specifically disclose a controller block in the form of a microprocessor which handles all the conversion between raw data and Ethernet, including processing of digital and analog signals, as well as all of the required code protocol translations, said microprocessor utilizing embedded software to manipulate the data signal to provide data to magnetics. However, *Hies et al.* discloses a controller block in the form of a microprocessor which handles all the conversion between raw data and Ethernet, including processing of digital and analog signals, as well as all of the required code protocol translations, said microprocessor utilizing embedded software to manipulate the data signal to provide data to magnetics (using a CPU to control routing table computations and performing protocol conversions from IPV4 to IPV6, see fig.6, co1.6 line 24 to col.7 line 58). The Patent Office states it would have been obvious to one of the ordinary skill in the art at the time the invention was made to implement *Hies et al.* teachings into the *Hovell et al. 's* converter to process data information because it would have allowed the master processor to efficiently perform routing computations, network diagnostics in a communication network (see *Hies'* co1.7 lines 2-23).

The Patent Office states that as to Claim 7, *Hovell et al.* discloses a communication protocol converter comprising: a housing defining first and second open cavities and a segregated interior chamber; each of said open cavities incorporating a plurality of electrical contacts positioned within said open cavities to form first and second connector ports wherein said first connector port is adapted to interface with a first communication protocol and said second connector port is adapted to interface with a second communication protocol (using network controller to process data conversion, see figs.1, 2, col.6 line 13 to co1.7 line 50); and at least one circuit board incorporating communication protocol conversion circuitry components disposed within said interior chamber in electrical communication with the electrical contacts of said first and second connector ports wherein said conversion circuitry bi-directionally translates

communication protocols (network protocol translation, see fig.2, col.7 line 17 to col.8 line 58), wherein the housing allows for the at least one circuit board to electronically communicate with both the first connector port and the second connector port and a microprocessor employing embedded software that converts Ethernet data from internet protocol version 4 to internet protocol version 6 (converting data from IPV4 to IPV6, see fig.2, col.7 line 17 to col.8 line 58).

Hovell et al. does not specifically disclose a microprocessor to receive Internet protocol 4 Ethernet data, removes the Internet protocol 4 header data, inserts Internet protocol 6 header data, recalculates the necessary Internet protocol header fields and outputs corresponding Internet protocol 6 Ethernet data. However, *Hies et al.* discloses a microprocessor receive Internet protocol 4 Ethernet data, removes the Internet protocol 4 header data, inserts Internet protocol 6 header data, recalculates the necessary Internet protocol header fields and outputs corresponding Internet protocol 6 Ethernet data (using a CPU to control routing table computations and performing protocol conversions from IPV4 to IPV6, see fig.6, col.6 line 24 to col.7 line 58). The Patent Office states it would have been obvious to one of the ordinary skill in the art at the time the invention was made to implement *Hies et al.'s* teachings into the *Hovell et al.'s* converter to process data information because it would have allowed the master processor to efficiently perform routing computations, network diagnostics in a communication network (see *Hies et al.'s* col.7 lines 2-23).

Hovell et al. discloses a tunnel is established across an IPv4 domain for the transport of packets from a source host on one IPv6 domain to a destination host on another IPv6 domain, there being respective interfaces between the IPv4 domain and the IPv6 domains.

Hies et al. discloses a method for providing handling of data sent between a first network and at least a second network and a third network, wherein the first network is of a first protocol and the at least second and third networks are of a second protocol at least partially overlap is provided. A packet transmitted from the first network is received. The packet has a first address prefix if the packet is directed to the second network and has a second address prefix if the packet is directed to the third network. A destination address of the packet and a source address of the packet are translated from the first protocol to the second protocol. The packet is directed to the second network if the packet has the first address prefix. The packet is directed to the third network if the packet has the second address prefix.

Amended Claim 1 requires a communication protocol converter comprising:(a) a first modular communication jack having: i) a housing defining an open cavity and a segregated interior chamber; ii) a connector port having a plurality of electrical contacts positioned within said open cavity; iii) at least one circuit board incorporating Ethernet to raw data conversion circuitry components for a first communication protocol disposed within said interior chamber in electrical communication with the electrical contacts of said connector port wherein the circuitry components are positioned on both sides of the at least one circuit board; and iv) a memory positioned on said circuit board in electrical communication with said conversion circuitry for a first communication protocol for receiving converted data whereby the memory is interconnected to a bi-directional data line that allows the input and output of raw data; (b) a second modular communication jack having: i) a housing defining an open cavity and a segregated interior chamber; ii) a connector port having a plurality of electrical contacts positioned within said open cavity; iii) at least one circuit board incorporating Ethernet to raw data conversion circuitry components for a second communication protocol disposed within said interior chamber in electrical communication with the electrical contacts of said connector port; iv) a memory positioned on said circuit board in electrical communication with said conversion circuitry for said second communication protocol for receiving converted data wherein the memory is interconnected with the bi-directional line to receive input of raw data from the first modular communication jack and further wherein said memory stores data utilized by a controller block; v) the controller block in the form of a microprocessor which handles all the conversion between raw data and Ethernet, including processing of digital and analog signals, as well as all of the required code protocol translations, said microprocessor utilizing embedded software to manipulate the data signal to provide data to magnetics wherein said controller block communicates with Ethernet through Ethernet interface; and (c) a bidirectional data interface electrically interconnecting said memory of said first communication jack with said memory of said second communication jack.

Amended claim 7 requires a communication protocol converter comprising: a housing defining first and second open cavities and a segregated interior chamber; each of said open cavities incorporating a plurality of electrical contacts positioned within said open cavities to form first and second connector ports wherein said first connector port is adapted to interface with a first communication protocol and said second connector port is adapted to interface with a

second communication protocol; at least one circuit board incorporating communication protocol conversion circuitry components disposed within said interior chamber in electrical communication with the electrical contacts of said first and second connector ports wherein said conversion circuitry bidirectionally translates communication protocols wherein the housing allows for the at least one circuit board to electronically communicate with both the first connector port and the second connector port; and a microprocessor employing embedded software that receives Internet protocol 4 Ethernet data; removes the Internet protocol 4 header data, inserts Internet protocol 6 header data, recalculates the necessary Internet protocol header fields and outputs corresponding Internet protocol 6 Ethernet data, the embedded software located on flash memory which is utilized by the microprocessor to perform its functions.

Neither *Hovell et al.* nor *Hies et al.* teach or suggest the control block as taught by the present invention. The Examiner in a previous communication admitted same, but now claims that the two cited references obviate the present invention. Although the applicant disagrees with the Examiner, applicant has amended the claims to more particularly point out the invention and distinguish same from the prior art. Applicant respectfully submits that the claims are now in condition for allowance. Notice to that effect is requested.

It is further submitted that the question under §103 is whether the totality of the art would collectively suggest the claimed invention to one of ordinary skill in this art. *In re Simon*, 461 F.2d 1387, 174 USPQ 114 (CCPA 1972).

That elements, even distinguishing elements, are disclosed in the art is alone insufficient. It is common to find elements somewhere in the art. Moreover, most if not all elements perform their ordained and expected functions. The test is whether the invention as a whole, in light of the teaching of the reference, would have been obvious to one of ordinary skill in the art at the time the invention was made. *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983).

It is insufficient that the art disclosed component's of Applicants' invention. A teaching, suggestion, or incentive must exit to make the combination made by Applicants. *Interconnect Planning Corp. v. Feil,* 774 F.2d 1132, 1143, 227 USPQ 543, 551 (Fed. Cir. 1988).

Applicant respectfully submits that this rejection overcomes based on the amendments to the independent claim for which this claim is based.

Claim 2-6 depend from Claim 1; Claims 8-11 depend from Claim 7. These claims are further believed allowable for the same reasons set forth with respect to independent Claims 1 and 7 since each sets forth additional novel steps of Applicant's Communication Protocol Converter and Method of Protocol Conversion.

We hereby request that the Commissioner withdraw extension fees due in connection with this response from Deposit Account No. 502191.

In view of the foregoing remarks, Applicant respectfully submits that all of the claims in the application are in allowable form and that the application is now in condition for allowance. any outstanding issues remain, Applicant urges the Patent Office to telephone Applicant's attorney so that the same may be resolved and the application expedited to issue. Applicant requests the Patent Office to indicate all claims as allowable and to pass the application to issue.

Respectfully submitted,
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